APPLICATION UNDER UNITED STATES PATENT LAWS

Atty. Dkt. No. PW 276570
(M#)

Invention: METHOD FOR FORMING A PHASE-SHIFTING MASK FOR SEMICONDUCTOR DEVICE MANUFACTURE

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- ☐ Reissue Application
- ☐ Plant Application
- ☒ Substitute Specification
  Sub. Spec Filed September 18, 2001
  in App. No. 09/886,984
- ☐ Marked up Specification re
  Sub. Spec. filed _____
  In App. No /

SPECIFICATION

METHOD FOR FORMING A PHASE-SHIFTING MASK FOR SEMICONDUCTOR DEVICE MANUFACTURE

Field of the Invention

The present invention relates to a method for forming a phase-shifting mask for the production of semiconductor devices and, more particularly, to a method for improving the lithographic resolution using a multi-transmittance phase-shifting mask

Description of the Prior Art

Generally, each level of semiconductor device circuitry is first generated on one or more photomasks that are, in turn, used in order to form the corresponding circuitry on a wafer surface. Typically, a series of reticles are generated in pattern generation works from the recorded circuit design data and, a master mask is then formed using the reticles. Attenuated phase-shifting masks used in DRAM fabricating processes, may be broadly classified into two types based on the way in which they are used. The first type is intended to increase the processing margin for forming linear spaces and the second is intended to increase the depth of focus for forming contact holes.

Figs. 1A and 1B provide plan and cross-sectional views illustrating conventional attenuated phase-shifting masks. The

upper figure is the cross-sectional view taken along the line A-A in the lower figure. In the drawings, chromium patterns 11 are formed on predetermined area of a quartz substrate 10. Further, Fig. 1A illustrates a conventional attenuated phase-shifting mask for forming fine patterns of lines and spaces with an expected processing margin.

Fig. 1B, however, illustrates a conventional attenuated phase-shifting mask for forming contact holes. The upper figure is the cross-sectional view taken along the line B-B in the lower figure. Generally, the chromium patterns designed and printed on the quartz substrate 10 are larger than the actual size of the pattern formed on a wafer. That is, the contact hole patterns are formed to provide a depth of focus (DOF) capable of resolving any size differences between mask pattern according to the design and the actual wafer-level patterns.

Fig. 1B shows an attenuated phase-shift mask having a transmittance of about 5 to 9% through the chromium patterns. If an amount of the transmittance level is a little high, interference may be generated by light transmitted through adjacent areas, thereby forming undesired patterns such as ghost images and side lobes. The use of the attenuated phase-shift mask with a low transmittance level, therefore, will tend to improve the resolution of fine patterns by suppressing the undesired patterns.

The size of the mask patterns may be also reduced in order to form correspondingly smaller patterns on the wafer,

but the degree to which the size of the mask pattern may be reduced will be limited by design rules associated with the mask forming processes. In particular, with the reduction of the size of the patterns, the processing margin can be reduced so dramatically that both a low transmittance mask and a high transmittance mask are required simultaneously to reproduce a single pattern with the desired accuracy. Accordingly, in those cases where only one mask, either a low transmittance mask or high transmittance mask, is used in the patterning process, the process performance is compromised. Indeed, the benefits of the non-selected mask are simply lost and the pattern produced will be less than optimal.

Summary of the Invention

It is, therefore, an object of the present invention to provide a method for improving resolution in the formation of photoresist patterns by using a multi-transmittance phase-shifting mask having both low transmittance and high transmittance regions.

It is another object of the present invention to improve the processing margin in fabricating semiconductor devices and improve the appearance of photoresist patterns and the resulting semiconductor devices.

In accordance with an aspect of the present invention, there is provided a method for forming a photomask for a semiconductor device, the method comprising the steps of:

forming a plurality of light blocking layers and a phase-shifting layer on a transparent substrate; defining at least two different areas that require different transmission levels in order to best pattern the semiconductor device; determining the necessary level of transmission of the exposing light based on the defined areas; and selectively patterning the light blocking layers and the phase-shifting layers using a photoresist layer as an etching mask to control transmittance of exposure light in the defined areas.

In accordance with another aspect of the present invention, there is provided a method for forming a photomask for a semiconductor device, wherein the semiconductor device has a scribe lane, a peripheral circuit area and a cell area, the method comprising the steps of: forming a first stacked structure on the a scribe lane with a first transmittance of 0% for the exposing light, wherein the first stacked structure includes a plurality of light blocking layers; forming a second stacked structure on the peripheral circuit area with a second transmittance for the exposing light, wherein the second stacked structure includes at least one light blocking layer and a phase-shifting layer; and forming a third stacked structure on the cell area with a third transmittance for the exposing light, wherein the third stacked structure includes at least two light blocking layers and a phase-shifting layer.

Brief Description of the Drawings

Other objects and aspects of the present invention will become apparent from the following description of the embodiments with reference to the accompanying drawings, in which:

Figs. 1A and 1B include plan and cross-sectional views illustrating conventional attenuated phase-shifting masks;

Fig. 2 illustrates a layout for a multi-transmittance phase-shifting mask according to an embodiment of the present invention;

Figs. 3A and 3B illustrate layouts of areas to which the multi-transmittance phase-shifting mask of Fig. 2 is applied; and

Figs. 4A to 4K are cross-sectional views illustrating a method for forming the multi-transmittance phase-shifting mask according to the present invention.

Detailed Description of the Preferred Embodiments

Hereinafter, the present invention will be described in detail referring to the accompanying drawings.

Fig. 2 illustrates a simple multi-transmittance phase-shifting mask on a quartz substrate according to an embodiment of the present invention comprising a scribe lane 30, a region having a transmittance of 0%, a peripheral circuit area 33, a

region having a high transmittance, and a cell area 32, a region having a low transmittance. As shown in Fig. 2, the phase-shifting mask according to the present invention has a different transmittance based on the desired characteristic of each area on the phase-shifting mask.

Fig. 3A illustrates a contact hole pattern in the peripheral circuit area in which contact hole 40 is a region having a transmittance of 100% without any phase-shifting or chromium layers. An outer area 42 surrounding the contact hole 40 is a region having a high transmittance, and an edge area 44 is a chromium pattern region having transmittance of essentially 0% for preventing undesired patterns resulting from side lobe effects.

Fig. 3B illustrates a contact hole pattern in a cell area in which contact holes 46 are regions having a transmittance of 100% without any phase-shifting or chromium layers. Fig. 3 also illustrates an outer area 45 comprising a region surrounding the contact holes 40 that has a low transmittance.

Figs. 4A to 4K are cross-sectional views illustrating a method for forming a multi-transmittance phase-shifting mask according to the present invention.

First, referring to Fig. 4A, a chromium layer 51a, a phase-shifting layer 52a, a chromium layer 53a, a chromium layer 54a and a first photoresist layer 55a are sequentially formed on a quartz substrate 50. The substrate, as illustrated, includes a scribe lane area (I), a peripheral circuit area (II) and a cell area (III). In a preferred

embodiment, the chromium layer 51a has transmittance of T1, the phase-shifting layer 52a, such as an oxide layer, has a phase difference of 180°, the chromium layer 53a has transmittance of T2 and the chromium layer 54a has transmittance of 0%.

Referring to Fig. 4B, a first photoresist pattern 55b is formed by applying an exposure and development process to the first photoresist layer 55a, thereby exposing predetermined portions of the chromium layer 54a.

Referring to Fig. 4C, predetermined portions of the quartz substrate 50 are then exposed by selectively etching the chromium layer 54a, the chromium layer 53a, the phase-shifting layer 52a and the chromium layer 51a, respectively, thereby forming chromium pattern 54b, chromium pattern 53b, phase-shifting pattern 52b and chromium pattern 51b.

Referring to Fig. 4D, after exposing portions of the quartz substrate 50, the photoresist pattern 55b is removed and, referring to Fig. 4E, a second photoresist layer 56a is formed on the resulting structure.

Referring to Fig. 4F, a second photoresist pattern 56b covering only the scribe lane area (I) exposing the peripheral circuit area (II) and the cell area (III), is then formed.

Next, referring to Fig. 4G, the exposed portion of chromium pattern 54b, i.e., those in the peripheral circuit area (II) and the cell area (III), are etched using the second photoresist pattern 56b as an etching mask to form chromium pattern 54c in the scribe lane area (I).

Referring to Fig. 4H, the second photoresist pattern 56b is then removed and, as illustrate in Fig. 4I, a third photoresist pattern 57 is formed in the scribe lane area (I) and the cell area (III), thereby exposing only the peripheral circuit area (II).

Referring to Fig. 4J, the portion of the chromium pattern 53b in the peripheral circuit area (II) is then etched using the third photoresist pattern 57 as an etching mask leaving only those portions of chromium pattern 53b that were formed in the scribe lane area (I) and the cell area (III) to form chromium pattern 53c.

Finally, referring to Fig. 4K, the photoresist pattern 57 is removed and a multi-transmittance phase-shifting mask according to the present invention is complete. In the multi-transmittance phase-shifting mask according to the present invention, a stacked structure in the scribe lane area (I) includes the chromium pattern 51b, the phase-shifting pattern 52b, the chromium pattern 53c and the chromium pattern 54c. The light transmission through this stacked structure in the scribe lane area (I) is T1*T2*T3 with a phase-shift of π and is sufficient to cut off the light transmission from the stepper light source and produce a transmittance of 0%. The stacked structure in the peripheral circuit area (II), however includes only the chromium pattern 51b and the phase-shifting pattern 52b so that the peripheral circuit area (II) has a high transmittance of T1 with a phase-shift of π. Similarly, the stacked structure in the cell area (III) includes the

chromium pattern 51b, the phase-shifting pattern 52b and the chromium pattern 53b so that the cell area (III) has a low transmittance of T1*T2 with a phase-shift of π.

As apparent from the above description, a phase-shifting mask according to the present invention provides a different light transmittance for different pattern areas such as the scribe lane, the peripheral circuit area and the cell area. This ability allows the transmittance to be tailored according to the desired characteristics of each area, thereby making such multi-transmittance masks highly compatible for the simultaneous formation of diverse elements on a semiconductor device. Accordingly, the present invention can suppress undesired patterns, such as ghost images and side lobe effects, and thereby improve the degree of integration of the semiconductor device and the production yield.

Although the preferred embodiments of the invention have been disclosed for illustrative purposes, those skilled in the art will appreciate that various modifications, additions and substitutions are possible, without departing from the scope and spirit of the invention as disclosed in the accompanying claims.